Max. Marks: 40+10
Time: 3hrs.

Unit-I

Number Systems: Binary, Octal, Hexadecimal number system and base conversions, Binary Arithmatic operations , 1's and 2's complement representation and there arithmetic. Binary codes-BCD, Grey, cyclic, ASCII, EBCDIC, Parity Bit Code, Unicode, Sequential Code.

Unit-II

Logic Gates and K-Map: AND, OR, NOT, XOR, XNOR, NOR, NAND (Definition, Symbols& Truth table). Boolean Algebra: Postulates, Duality Principal, De Morgan's Law, Simplification of Boolean Identities, Standard SOP & POS Forms, Simplification using K-map, don't care condition implementation of SOP & POS form using NAND and NOR Gate.

Unit III

Logic Families-I: - Unipolar & Bipolar Logic families, Characteristics of Digital IC's. (fan in, fan out, propagation delay, Noise Margin, level of Gating), Resistance Transistor Logic RTL(NOR), Direct Coupled Logic(DCTL), Diode Transistor Logic, High Threshold Logic HTL,DTL (NAND).

Unit-IV

Logic Families-II: - TTL, Schott-key TTL, MOS logic, CMOS Logic Gate (NAND, NOR).

Reference Books:

1. Digital Electronics by R.P. Jain

Note:

1. Syllabus in each Theory Paper is divided in 4 units.
    I. A Student is required to attempt 5 questions in all.
    II. Question No 1 is compulsory, consisting of short answer type questions based on all the 4 units.
    III. Two questions will be set from each unit. A student is required to attempt one question from each unit.
    IV. All questions carry equal marks.
2. Use of simple calculator is permissible.
3. Instructions should be imparted using SI system of units. Familiarity with CGS system of units should also be ensured.
4. Distribution of Marks: 40+10*= 50.
    * Each question paper will be of 40 marks and 10 marks in each theory paper are awarded through internal assessment in each semester.
5. Work load – 3 periods per week per theory paper.