Session: 2023-24			
Part A - Introduction			
Subject	ELECTRONICS		
Semester	FIRST		
Name of the Course	Basic Digital Electronics		
Course Code	B23-ELE-103		
Course Type: (CC/MCC/MDC/CC-M/DSEC/VOC/DSE/PC/AEC/VAC)	**CC-M1**		
Level of the course	100-199		
Pre-requisite for the course (if any)	Physics as a Subject at 4.0 Level (Class XII)		
Course Learning Outcomes (CLO):	After completing this course, the learner will be able to: 1. To understand the basics of various Number systems and their conversions 2. To understand the basics of Boolean algebra and its theorems 3. To understand the concept and basics of different logic gates 4. To understand the concept and minimization techniques using K-maps 5. To learn and understand the use of various electronic components and equipment's used for analysis of basic digital electronic circuits		
Credits	Theory	Practical	Total
	1	1	2
Contact Hours	15	30	45
Max. Marks: 50 (30 Theory + 20 Practical) **Internal Assessment Marks: 10 Theory + 5 Practical** **End Term Exam Marks: 20 Theory + 15 Practical**		**Exam Time: 3 Hours each for Theory & Practical**	

Part B- Contents of the Course

Instructions for Paper- Setter

1. Nine questions will be set in all. All questions will carry equal marks.
2. Question No. 1, which will be short answer type covering the entire syllabus, will be compulsory. The remaining eight questions will be set unit wise selecting two questions from each Unit I to IV. The candidate will be required to attempt question No. 1 and four more questions selecting one question from each unit.

Unit	Topics	Contact Hours
I	**Number Systems:** Introduction to Decimal, Binary, Octal, Hexadecimal Number Systems and their inter-conversions; BCD codes, Excess-3 codes, Gray codes, code conversions, binary arithmetic (addition, Subtraction, multiplication, division), 1's and 2's compliments and 9's and 10's compliments.	3
II	**Boolean Algebra:** Postulates & theorems of Boolean algebra, Duality Principle, De-Morgan's Theorem.	4
III	**Logic Gates:** Positive and Negative Logic, Basic Logic Gates: AND, OR, NOT (symbol, truth-table, circuit diagram, working); NAND, NOR, EX-OR, EX-NOR (symbol, truth table).	4
IV	**Minimization Techniques:** Reduction of Boolean expressions using Boolean Identities, SOP and POS form of Boolean functions, Karnaugh Map simplifications, implementations of SOP and POS form using NAND and NOR gates.	4
V*	**Note:** A candidate is required to perform minimum 4 experiments out of the list provided during course of study in this semester. 1. Design of basis logic gates using discrete components. 2. Study of different type of digital IC's :(functions, pin diagram, block diagram of various Digital ICs etc.). 3. Data Sheet Analysis of Digital ICs (Quote the data sheet of any two digital ICs in Laboratory File). 4. Realization of Boolean Identities on Digital Trainer Kit. 5. Digital trainer using AOI. 6. Digital trainer using NAND gates. 7. Realization of K-map expression on Digital Trainer Kit.	30

Suggested Evaluation Methods

Internal Assessment: ➢ **Theory 10 Marks** • Class Participation: **4 Marks** • Seminar/presentation/assignment/quiz/class test etc.: • Mid-Term Exam: **6 Marks** ➢ **Practicum 5 Marks** • Class Participation: • Seminar/Demonstration/Viva-voce/Lab records etc.: **5 Marks** • Mid-Term Exam:	**End Term Examination:** **20 Marks** **15 Marks**

Part C-Learning Resources

Recommended Books/e-resources/LMS:

1. Digital Electronics by R.P. Jain
2. Digital Computer Electronics by A. P. Malvino